Amendments to the Specification:

Please replace the paragraph on page 5, lines 20-26 with the amended paragraph:

FIG. 4 shows one embodiment of a head and tail caching system 400 constructed in accordance with the present invention. The system 400 includes a FIFO circuit 402, a controller 404, and a memory 406. The FIFO circuit 402 includes a tail FIFO memory ~~408~~ 410, a head FIFO memory ~~410~~ 408 and a multiplexer (mux) 412. In one embodiment, the tail and head FIFOs have 256 bytes of memory for data storage. However, the FIFOs may be of any size depending on the caching application. The mux 412 has two inputs that can each be selectively coupled to a mux output.

Please replace the paragraph on page 11, lines 9-14 with the amended paragraph:

At block 814, a determination is made whether the fill level of the head FIFO will allow data blocks to be transferred from the memory to the head FIFO. If there is not enough space available in the head FIFO, the method proceeds to block ~~812~~ 810, where blocks of data continue to form in the tail FIFO. If there is enough space in the head FIFO, the method proceeds to block ~~818~~ 816. For example, the controller 404 makes this determination from the head FIFO fill indicator 422.